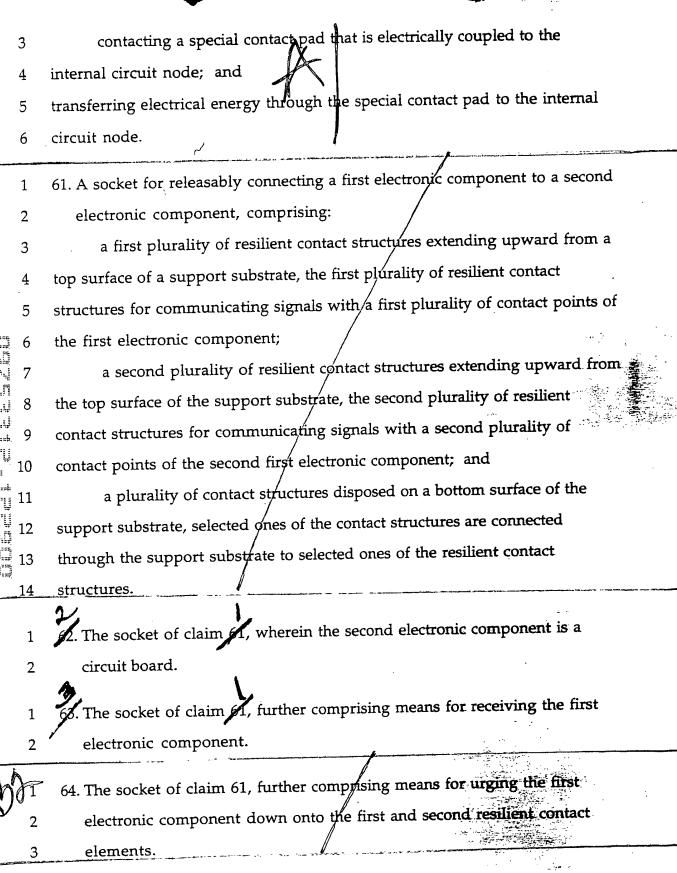


CLAIMS

What is claimed is:

- 1 1. An integrated circuit comprising:
- 2 circuitry;
- a bond pad coupled to the circuitry and for interfacing the circuitry with
- 4 an external circuit; and
- a special contact pad coupled to the circuitry, the special contact pad for
- 6 use only when testing the circuitry.
- 1 2. The integrated circuit of claim , wherein the special contact pad is smaller
- 2 than the bond pad.
- 1 3. The integrated circuit of claim , wherein the special contact pad has a
- 2 maximum dimension of approximately 10 microns.
- 1 4. The integrated circuit of claim 1, wherein the special contact pad is
- 2 structured to receive a spring contact element.
- 1 5. The integrated circuit of claim 1, wherein the special contact pad is for
- 2 communicating test data to the circuitry.
- 1 6. The integrated circuit of claim 1, wherein the special contact pad is for
- 2 communicating data from the circuitry.
- 7. The integrated circuit of claim 1, wherein the special contact pad is for
- 2 contacting a circuit node internal to the circuitry.
- 1 8. An integrated circuit comprising:
- 2 a plurality of circuits;



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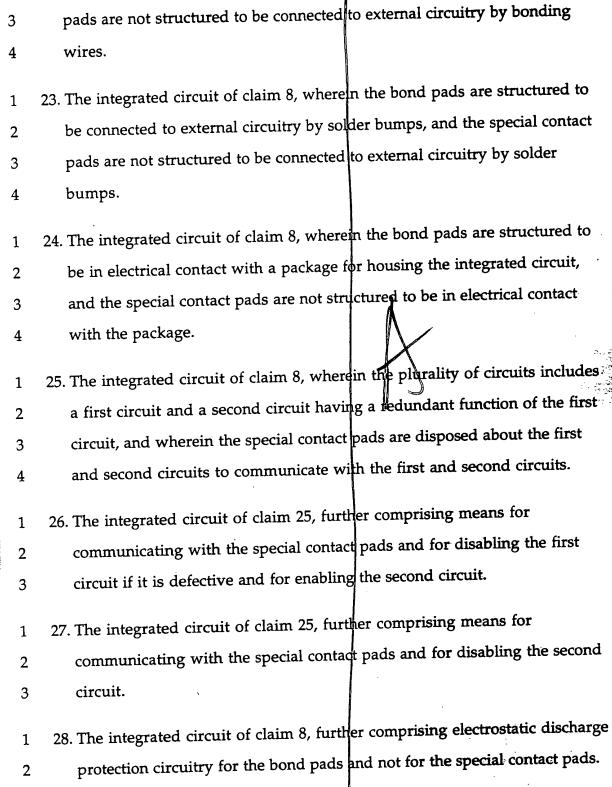
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3	a plurality of bond pads each coupled to at least one of the plurality of
4	circuits, the plurality of bond pads for interfacing the plurality of circuits with
5	circuits external to the integrated circuit; and
6	a plurality of special contact pads each coupled to at least one of the
7	plurality of circuits and providing an electrical contact for communicating
8	with the plurality of circuits.
1	9. The integrated circuit of claim 8, wherein the bond pads are arranged in a
2	first predetermined alignment and the special contact pads are arranged in
3	a second predetermined alignment.
1	10. The integrated circuit of claim 8, wherein the bond pads are disposed along
2	the periphery of the integrated circuit, and a least one of the special
3	contact pads is not disposed on the periphery of the integrated circuit.
1	11. The integrated circuit of claim 8, wherein the bond pads are aligned in a
2	grid pattern on the integrated circuit, and at least one of the special contact
3	pads is not aligned in the grid pattern.
1	-12. The integrated circuit of claim 8, wherein the bond pads are aligned in a
2	lead-on-center configuration, and at least one of the special contact pads is
3	not aligned in the lead-on-center configuration.
. 1	13. The integrated circuit of claim 8, wherein the special contact pads are
2	smaller than the bond pads.
1	14. The integrated circuit of claim 8, further comprising a spring contact
2	element attached to one of the special contact pads.

- 15. The integrated circuit of claim 8, wherein at least one of the special contact
 pad is electrically disposed between two of the plurality of circuits to
- 3 monitor signals transmitted between circuits.
- 1 16. The integrated circuit of claim 8, wherein one of the special contact pads
- 2 communicates test data to one of the circuits, and another one of the
- 3 special contact pads communicates an output of the circuit.
- 1 17. The integrated circuit of claim 8, wherein one of the special contact pads
- 2 communicates test data to the one of the circuits, and one of the bond pads
- 3 communicates an output of the circuit.
- 1 18. The integrated circuit of claim 8, wherein one of the bond pads
- 2 communicates test data to one of the circuits and one of the special contact
- 3 pads communicates an output of the circuit.
- 1 19. The integrated circuit of claim 8, wherein in a first mode of operation one
- of the special contact pads communicates data to one of the circuits, and in
- 3 a second mode of operation the special contact pads communicates data
- 4 from the circuit.
- 1 20. The integrated circuit of claim 8, wherein one of the plurality of circuits is
- an embedded memory array, and the special contact pads communicates
- address and test data to the embedded memory array.
- 21. The integrated circuit of claim 8, wherein one of the plurality of circuits
- 2 includes programmable circuitry, and the special contact pads are for
- 3 communicating signals for programming the programmable circuitry.
- 22. The integrated circuit of claim 8, wherein the bond pads are structured to
- 2 be connected to external circuitry by bonding wires, and the special contact

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29. An integrated circuit comprising:

a plurality of bond pads;

3	an internal circuit not directly monitorable by the bond pads; and
4	at least one special contact pad for directly accessing the internal circuit
1	30. The integrated circuit of claim 29, wherein the internal circuit comprises
2	an embedded memory array, and the at least one special contact pad
3	communicates address and memory data with the embedded memory
4	агтау.
1	31. The integrated circuit of claim 29, wherein the internal circuit comprises
2	programmable circuitry, and the at least one special contact pad
3	communicates programming signal to the programmable circuitry.
1	32. The integrated circuit of claim 29 wherein the bond pads are arranged in a
1 2	first predetermined alignment and the at least one special contact pad is in
₩ 3	a second predetermined alignment.
TU " 1	33. The integrated circuit of claim 29 wherein the at least one special contact
1 2 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	pad is smaller than the bond pads.
1	34. The integrated circuit of claim 29, further comprising a spring contact
2	element attached to the at least one special contact pad.
1	35 A package for housing an integrated circuit, comprising:
2	a plurality of terminals for testing the overall operation of the
3	integrated circuit; and
4	a special contact pad for directly accessing an internal circuit of the
5	integrated circuit.
1	36. The package of claim 35, wherein the special contact pad is for
2	communicating test signals for the integrated circuit.



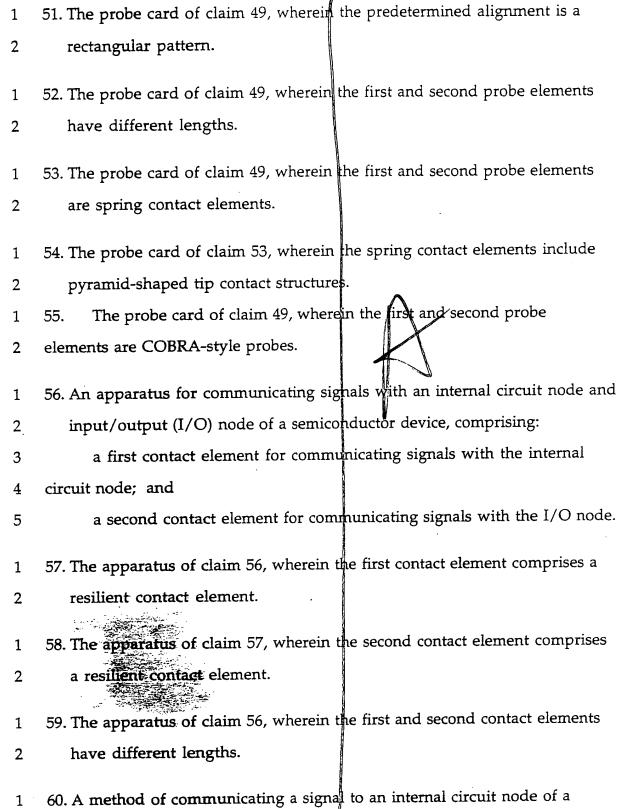
1	37. The package of claim 35, wherein the special contact pad is for
2	communicating test signals from the integrated circuit.
1	38. The package of claim 35, wherein the contact pads are aligned in a grid
2	pattern on the integrated circuit, and the special contact pads is not aligned
3	in the grid pattern.
1	39. The package of claim 35, wherein the package comprises a ball-grid-array
2	(BGA) package and the contact pads include contact balls.
1	40. The package of claim 35, wherein the special contact pad is smaller than
2	the contact pad.
1	41. The package of claim 35, wherein the special contact pad has a maximum
2	dimension of approximately 10 microns.
1 ·	42. A method of testing circuitry in an integrated circuit having bond pads
2	and a special contact pad, the method comprising:
3	providing test signals to the circuitry; and
4	monitoring an output of the circuitry through the special contact pad.
1	43. A method of testing circuitry in an integrated circuit having bond pads
2	and a special contact pad, the method comprising:
3	providing test signals to the circultry through the special contact pad;
4	and and a second and
5	montaining an output of the circuitry through the bond pad.
1	44. A method of testing an integrated circuit having bond pads and a special
2	contact pad, the method comprising
3	providing test signals to a first circuit through at least one of the bond
4	pads;

	5	monitoring an output of the first circuit through the special contact
	6	pad;
	7	providing the output of the first circuit to a second circuit; and
	8	providing an output of the second dircuit to at least another one of the
	9	bond pads.
	1	45. A method of testing an integrated circuit on a wafer, comprising:
	2	electrically contacting a first test substrate to special contact pads
	3	disposed on the integrated circuit; and
	4	electrically contacting a second test substrate to bond pads disposed on
	5	the integrated circuit.
	1	46. A probe card comprising:
	1	
	2	a first probe element for contacting bond pads of an integrated circuit;
	3	and and a special contact pad of the
	4	a second probe element for contacting a special contact pad of the
	5	integrated circuit
	1	47. The probe card of claim 46, wherein the first and second probe elements
		comprise cantilevered probes.
	2	comprise carmevered probes.
	1	48. The probe card of claim 46, wherein the first and second probe elements
	2	comprise contact balls.
	1	49. The probe card of claim 46, further comprising a plurality of the first probe
	1	u
	2	elements arranged in a first predetermined alignment, and wherein the
	3	second probe element is arranged in a second predetermined alignment.
	1	50. The probe card of claim 49, wherein the predetermined alignment is a grid

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pattern.

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semiconductor device, comprising: